IN THE SPECIFICATION:

Please amend paragraph **[0001]** and the title immediately preceding it as follows:

~~Related Application~~CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of ~~pending U.S. App. Ser.~~ United States patent application Serial No. 09/146,108, filed ~~Sep.~~ September 3, 1998, now U.S. Patent 6,780,758, issued August 24, 2004.

Please amend paragraph **[0006]** as follows:

[0006] FIGS. 1A through 1C depict an in-process semiconductor device as is known in the ~~art.~~ art;

Please amend paragraph **[0007]** as follows:

[0007] FIG. 2 illustrates a known configuration for a container cell ~~capacitor.~~ capacitor;

Please amend paragraph **[0008]** as follows:

[0008] FIGS. 3, 4A through 4D, 5A through 5C, 6, and 7A through 7B represent steps that are taken in various exemplary method embodiments of the current ~~invention.~~ invention;

Please amend paragraph **[0009]** as follows:

[0009] FIG. 8 is a process flow diagram organizing the steps depicted in FIGS. 3, 4A through 4C, 5A through 5C, 6, and 7A ~~through 7B.~~ through 7B;

Please amend paragraph **[0010]** as follows:

[0010] FIGS. 9A through 9E show one preferred exemplary embodiment of the current ~~invention.~~ invention;

Please amend paragraph **[0011]** as follows:

[0011] FIGS. 10A through 10D illustrate a damascene process as known in the art. FIGS. 10E and 10F demonstrate the known way to complete an interconnect structure that began

with the damascene process in FIGS. 10A-10D. FIG. 10G represents another exemplary embodiment of the current ~~invention.~~ invention;

Please amend paragraph **[0012]** as follows:

[0012] FIG. 11 is yet another exemplary embodiment of the current ~~invention.~~ invention; and

Please amend paragraph **[0014]** as follows:

[0014] FIG. 1A depicts a portion of an in-process semiconductor device that, to this point, has been created by steps known in the art. An insulation layer 20 defines an opening 22, the bottom of which is generally level with the top of a portion of conductive material 24 that continues deeper into the insulation layer 20 disposed over substrate 50. The portion in FIG. 1A could be understood to represent one of several device portions at various stages of fabrication. For purposes of explanation, it will be assumed throughout most of the following discussion that FIG. 1A represents a portion of a memory cell, wherein opening 22 is actually a container 26, seen in FIG. 1B, designating the site where a capacitor will be formed. It follows then that the conductive material 24 in FIG. 1A can be more specifically identified as a poly plug 28 in FIG. 1B. Further, the insulating layer 20 is assumed to be an oxide 30, most likely silicon dioxide. Moreover, it is not necessary that one continuous insulation layer envelop the sides of both the container 26 and the poly plug 28. As seen in FIG. 1C, a second insulation layer 32 surrounds the sides of the poly plug 28 and defines the bottom of the container 26, while the oxide 30 defines the sides of the container 26. This is, in fact, the layering scheme that will occur if the process follows as described above in the background section. In addition, it is not necessary to use an oxide for the second insulation layer 32. In fact, it is preferable in the current invention if the second insulation layer 32 comprises a nitride at least around the poly plug 28, as this will help protect the poly plug 28 from oxidation during subsequent process steps. It should further be noted that, in illustrating a container cell/plug portion of a semiconductor device, it is understood that the poly plug 28 fills a hole extending down through the second insulation layer 32 and contacting the surface of the substrate 50, as seen in FIG. 1C. In the current

application, the term "substrate" or "semiconductor substrate" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term "substrate" also refers to any supporting structure including, but not limited to, the semiconductive substrates described above.

Please amend paragraph **[0017]** as follows:

[0017] Returning to the container cell/plug example, prior art teaches further processing as depicted in FIG. 2. A conductive material is layered along the sides and bottom of the container 26 to serve as a bottom plate 34, which in this case will be the storage node. A dielectric layer 36 is formed over the bottom plate 34, and another conductive material is layered over the dielectric layer 36 to form the top plate 38 which, in this embodiment, is the cell plate of the capacitor 40. Planarization and patterning of these layers 34, 36, and 38 are carried out as needed.

Please amend paragraph **[0019]** as follows:

[0019] The next step comprises providing an initial barrier component 42 over the poly plug 28. This material is designated as an initial barrier component because, while initially it may not act as a diffusion barrier, the material at least contains components that can be used to create a barrier to the diffusion of silicon. In a preferred embodiment shown in FIG. 4A, the initial barrier component 42 is the result of selectively depositing titanium through chemical vapor deposition (CVD) onto the poly plug 28. The CVD process can be carried out under the following exemplary parameters: $TiCl_4$ for a source gas; H_2 for a reactive gas, wherein the flow rate of H_2 may be 2-10 times that of $TiCl_4$; Ar or He for carrier gasses; a substrate temperature of around ~~400 degrees C;~~ 400°C; a reaction chamber pressure ranging from 0.2 to 2 torr; with ~~an rf~~ an RF voltage applied to the reaction chamber. *See, e.g.*, ~~United States Patent Number~~ U.S. Patent No. 5,173,327 ~~by~~ to Sandhu et al. As a result of the selective CVD process, a layer of titanium will deposit only on the poly plug 28. The temperatures reached during the process,

however, are sufficient to cause the titanium to react with the silicon in the poly plug 28 to form titanium silicide ($TiSi_X$, where x is a positive number). It is possible to deposit relatively unreacted titanium onto the poly plug 28 at low enough temperatures, and the current invention certainly includes such a process and apparatus within its scope. However, it is actually preferable under the current invention to have a silicide layer above the poly plug 28, as such a layer will enhance electrical contact between the poly plug 28 and any overlying conductive material. Thus, if providing an initial barrier component 42 does not inherently result in an electrical contact enhancement material, then it is preferred that an additional step be taken to create such a material. Such a step is described further below, but for now, it is assumed that the selectively deposited initial barrier component 42 underwent silicidation during deposition, thereby forming an electrical contact enhancement layer 48 above the poly plug 28, as seen in FIG. 4B. Specifically, the ~~CVD'd~~ titanium deposited by chemical vapor deposition underwent silicidation during CVD to form $TiSi_X$.

Please amend paragraph **[0021]** as follows:

[0021] It should be understood, however, that the initial barrier component 42 could comprise a different material as long as that material, either as initially deposited or with further processing, will help protect against the diffusion of silicon. Such materials include tungsten; rhenium; platinum group metals including platinum, palladium, iridium, ruthenium, rhodium, and osmium; oxides of those Pt-group metals, such as ruthenium oxide (RuO_X, where x is a non-negative number, preferably 2); alloys of those Pt-group metals; and transition metal borides including TiB. Titanium is a preferred material because it is relatively easy to selectively deposit. Nevertheless, using ruthenium oxide for the initial barrier component 42 is an alternative preferred embodiment. As discussed below, it is sometimes desirable to provide a layer above the poly plug 28 to protect it from oxidation. For such a layer, selective deposition is not necessary. In some embodiments, this requires a layer in addition to the diffusion barrier. Ruthenium oxide, however, may have the benefit of acting as both a barrier against silicon diffusing from the poly plug 28 as well as a barrier against oxygen that might otherwise reach the poly plug 28. Accordingly, if ruthenium oxide is the material of choice for the initial barrier

component 42, as shown in FIG. 4D, then that material may serve as both the diffusion barrier 44 and the oxidation protection layer 46. One skilled in the art may then proceed to forming the capacitor 40, comprising layers 34, 36, and 38, in the manner described above. The ruthenium oxide will serve as an ~~interface—a common boundary—between~~ interface, a common boundary, between the two conductive elements which, in this case, are the poly plug 28 and the bottom plate 34. Again, planarization of the layers, including the diffusion barrier 44/oxidation protection layer 46, as well as patterning steps, are carried out as needed. Similarly, if iridium is chosen for the initial barrier component 42, it, too, may act as both the diffusion barrier 44 and the oxidation protection layer 46 shown in FIG. 4D. Moreover, any material from the platinum metal group (including platinum, rhodium, palladium, and osmium) and their corresponding metal oxides may also serve dual roles as a diffusion barrier 44 and an oxidation protection layer 46.

Please amend paragraph **[0022]** as follows:

[0022] Thus selectivity, while preferred in certain embodiments, is not a necessary requirement under the current invention. It may be more desirable in some embodiments to deposit a conformal initial barrier component 42 and then pattern the initial barrier component so that it remains only over the poly plug 28, as illustrated in FIG. 4A. Alternatively, it is possible to allow the conformally deposited initial barrier component 42 to remain as a lining along the container 26, as shown in FIG. 4C, with a planarization step taken if it is necessary to restrict the initial barrier component 42 to within the container 26. If tungsten is used as the initial barrier component 42, for example, CVD parameters would include using WF_6 and H_2 as precursors at ~~450 degrees C~~ 450°C and at a pressure of 80 torr. *See, e.g.*, ~~United States Patent~~ U.S. Patent No. 5,654,222 ~~by~~ to Sandhu et al.

Please amend paragraph **[0023]** as follows:

[0023] Returning to the preferred embodiment in which titanium silicide is used as the electrical contact enhancement layer 48, the process moves from the step depicted in FIG. 4A to a nitridation step, the result of which is illustrated in FIG. 5A. It is preferred that the nitridation

be carried out using an N_2/H_2 plasma. Parameters for this process include a temperature of around 600 to ~~675 degrees Celsius,~~ 675°C, a pressure of about 1 torr, a power of about 500 watts, and a flow rate generally ranging from 10 to 1000 sccm for the N_2 and H_2 gasses. This process continues until a titanium nitride (TiN) layer about 50 angstroms thick is created from the initial barrier component 42. This results in having nitridized about one-half of the electrical contact enhancement layer 48. As seen in FIG. 5A, the TiN layer serves as one embodiment of the diffusion barrier 44 sought under the current invention. While alternate embodiments of the current invention may call for fully nitridizing the initial barrier component 42, as seen in FIG. 5C, it is preferred to retain a portion of un-nitridized titanium silicide for improved electrical communication. In embodiments where the initial barrier component 42 has yet to become an electrical contact enhancement layer 48, it is still preferable to retain an un-nitridized portion of that layer, as it can later become an electrical contact enhancement layer 48 in a step described below. Regardless of the particular depth of the nitride, that material acts as a barrier to silicon, which has a tendency to diffuse from the poly plug 28 into the capacitor that is to be constructed in the container. Using a plasma process for nitridation is preferred because it can be done *~~in-situ~~* ~~in~~ *situ*, in relatively the same environment where the initial barrier component 42 was deposited. This reduces the risk of exposing the in-process device to contaminants.

Please amend paragraph **[0024]** as follows:

[0024] Nevertheless, other nitridation methods fall within the scope of the current invention. Such methods include a thermal process such as an N_2/NH_3 anneal. This method would most likely be used if tungsten served as the material for the initial barrier component. In this case, the tungsten could be exposed to an N_2/NH_3 ambient under a pressure of approximately 4.5 torr and having a temperature of about ~~360 degrees C.~~ 360°C. Further, approximately 350 W of RF power could be applied to generate plasma from the gasses, which can occur in an N_2:NH_3 ratio ranging from 2:1 to 50:1. As for duration, this anneal process continues until the desired amount of tungsten nitride has been formed from the initial barrier layer. Thus, if the initial barrier component 42 is made of tungsten and covers only the poly plug 28, as in FIG. 4A, the nitridation step creates a tungsten nitride diffusion barrier 44, as represented in FIG. 5A. If, on

the other hand, the initial barrier component 42 was a conformal layer of tungsten, represented by FIG. 4C, then the nitridation step would result in a conformal layer of tungsten nitride serving as the diffusion barrier 44. This is demonstrated in FIG. 5B, wherein the initial barrier component 42 has been partially nitridized. Further, if the initial barrier component 42 is made of ruthenium or any other Pt-group metal, the nitridation processes described above as well as others known in the art can be used to form a nitride diffusion barrier 44.

Please amend paragraph **[0026]** as follows:

[0026] However, it is preferred in other embodiments to further develop the interface. If silicidation has not occurred by this point in the process, such a step may be performed now. As discussed above, this enhances the electrical contact between the poly plug 28 and the capacitor that will be constructed thereover. Assuming that (1) generally unreacted titanium has been selectively deposited as the initial barrier component 42, and (2) only the top 50 angstroms of the titanium has been nitridized, then at this step in this particular embodiment, the remaining 50 angstroms of titanium are changed into titanium silicide. Silicidation can be conducted using any known method but is preferably performed using a rapid thermal anneal process at about ~~650 degrees C~~ 650°C for as long as necessary to achieve the desired amount of $TiSi_X$. The result of this process is depicted in FIG. 6: a $TiSi_X$ layer that acts as an electrical contact enhancement layer 48 is formed under the diffusion barrier 44. The formation of this electrical contact enhancement layer 48 helps to counteract the effects of any oxide within the poly plug 28 that has developed up to this point. Much of this oxidation occurs at the top of the poly plug 28. Thus, although a 50 angstrom measurement is used as an example thickness of the electrical contact enhancement layer 48, it is preferred that enough silicon in the poly plug 28 be reacted during silicidation so that a relatively oxide free portion of the poly plug 28 remains. This silicidation process may also be used in other embodiments, including those using unreacted tungsten as the initial barrier component 42, wherein silicidation will result in an electrical contact enhancement layer 48 made of tungsten silicide (WSi_X). Alternatively, silicidation of a ruthenium initial barrier component 42 will result in an electrical contact enhancement layer 48 made of ruthenium silicide. Similarly, if the initial barrier component 42 is rhenium or any Pt-group metal,

silicidation will result in an electrical contact enhancement layer 48 comprising a silicide of the original material.

Please amend paragraph **[0027]** as follows:

[0027] Still another step that could be performed includes providing an oxidation protection layer 46, which helps protect the poly plug 28 from oxidation during further processing. In several embodiments, this step involves the CVD of a metal, such as rhenium or the Pt-group metals. Alternatively, an oxide of these metals could be used for this layer 46. As another option, an alloy comprising a selection of the metals listed above could be used. As an example of this step, the CVD of ruthenium can be accomplished with a substrate temperature ranging from about 225 to ~~325 degrees Celsius~~ 325°C (more preferably ~~250 degrees C)~~ 250°C) and a pressure of around 3 torr (more preferably 1 torr). Precursor chemistries include organoruthenium complexes, such as bis(cyclopenta-dienyl) ruthenium ($Ru(C_5H_5)_2$), triruthenium dodecacarbonyl ($Ru_3(CO)_{12}$), tricarbonyl (1,3-cyclohexadiene) ruthenium, and the like. Alternatively, a halogenated compound, such as ruthenium tetrachloride ($RuCl_4$), $RuCl_3$, or RuF_5 could be used. The CVD of ruthenium oxide involves a similar reaction but requires a lower ~~temperature around 150 degrees C due~~ temperature, around 150°C, due to the addition of oxygen to the reaction.

Please amend paragraph **[0029]** as follows:

[0029] For purposes of clarity, FIGS. 9A through 9E reiterate a preferred embodiment of the current invention. A low surface for the poly plug 28 is provided as depicted in FIG. 9A. In FIG. 9B, an initial barrier component 42 including titanium is selectively deposited through CVD. The deposition conditions cause the titanium to react with the silicon in the poly plug 28 to form titanium silicide, thereby allowing the initial barrier component 42 to act as an electrical contact enhancement layer 48. FIG. 9C demonstrates that the top portion of the electrical contact enhancement layer 48 is subsequently nitridized to form the diffusion barrier 44. Next, an oxidation protection layer 46 made of ruthenium or ruthenium oxide is conformally layered within the container 26 and over the diffusion barrier 44, as seen in FIG. 9D. With the

completion of the ~~interface comprising layers 44, 46, and 48 prior~~ interface, comprising layers 46, 48 and barrier 44, prior art steps may then be resumed, such as those depicted in FIG. 9E, involving layering the bottom plate 34, dielectric layer 36, and top plate 38 of a capacitor 40 over the oxidation protection layer 46. Planarization may also be performed as appropriate.

Please amend paragraph **[0032]** as follows:

[0032] One skilled in the art can appreciate that, although specific embodiments of this invention have been described above for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. For example, FIG. 11 depicts an embodiment wherein the poly plug 28 is not recessed. As another example, shown in FIG. 12A, it is not necessary that the diffusion barrier 44 and the electrical contact enhancement layer 48 originate from the same material. In this example, the electrical contact enhancement layer 48 results from the silicidation of a ~~selectively CVD'd~~ titanium layer selectively deposited by CVD. The diffusion barrier 44, on the other hand, comes from nitridizing a tungsten layer that is over only the poly plug 28. Similarly, the diffusion barrier 44 in FIG. 12B comes from nitridizing a tungsten layer that conforms to the container 26 and overlies the $TiSi_X$ electrical contact enhancement layer 48. Moreover, the current invention can be used in any situation wherein silicon is used to make an electrical contact. In addition, it should be noted that the invention becomes more beneficial as the silicon contact area decreases in size. Further, the end product and in-process versions of the product are also included within the scope of this invention. Finally, one skilled in the art can appreciate that the cross sections depicted the figures are not to scale. Rather, particular elements, such as the layers discussed above, are sized to clearly indicate embodiments of the current invention. Accordingly, the invention is not limited except as stated in the claims.